

Design, Construction and Operation of a Low-Power, Autonomous Radio-Frequency Data-Acquisition Station for the TARA Experiment

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Abstract

Employing a 40-kW, 54.1 MHz radio-frequency transmitter just west of Delta, UT, the TARA (Telescope Array RADar) experiment seeks radar detection of extensive air showers (EAS) initiated by ultra-high energy cosmic rays (UHECR). For UHECR with energies in excess of 10^{19} eV, the Doppler-shifted “chirps” resulting from EAS shower core radar reflections should be observable above background (dominantly galactic) at distances of tens of km from the TARA transmitter. In order to stereoscopically reconstruct cosmic ray chirps, two remote, autonomous self-powered receiver stations have been deployed. Each remote station (RS) combines both low power consumption as well as low cost. Triggering logic, the powering and communication systems, and some specific details of hardware components are discussed.

Keywords: cosmic ray, FPGA, radar, digital signal processing, chirp

1. Introduction

Within the last 30 years, the sub-field of ultra-high energy cosmic ray (UHECR; $E > 10^{18}$ eV) astronomy has emerged as a vibrant experimental and theoretical sub-field within the larger field of particle astrophysics, comprising studies of both charged and neutral particles at macroscopic kinetic energies. The physics interest in UHECR lies in understanding i) the nature of the cosmic accelerators capable of producing such enormously energetic particles at energies millions to billions of times higher than we are capable of producing in our terrestrial accelerators, ii) the details of the interaction of UHECR with the cosmic ray background, evident in the observed energy spectrum of cosmic rays as an upper ‘cut-off’[1], or maximum observed energy, at approximately 10^{20} eV, and iii) correlations in the arrival directions of UHECR with exotic objects such as neutron stars, gamma-ray bursts (GRB), and active

galactic nuclei (AGN). Experimentally, charged-particle UHECR astronomy is currently dominated by two experiments – the Southern Hemisphere Pierre Auger Observatory (PAO)[2] based in Malargue, Argentina and the Northern Hemisphere Telescope Array (TA)[3] based in Utah, USA. The construction of these observatories is very similar, based on a large number of ground detectors sampling the charged component of Extensive Air Showers (EAS) and deployed over hundreds of square kilometers at ~ 1 km spacing, coupled with a much smaller number of atmospheric nitrogen fluorescence detectors having a much more restricted duty cycle, but individually capable of providing a more comprehensive image of atmospheric shower development. Within the last decade, the PAO has been complemented by an array of radio-wave antennas, capable of measuring the signal generated primarily by the separation of the charged particles comprising the down-moving air shower in the geomagnetic field[4].

The TARA experiment (Telescope Array RADar) attempts to achieve large aperture for EAS detection by bi-static observation of radar reflections from the core

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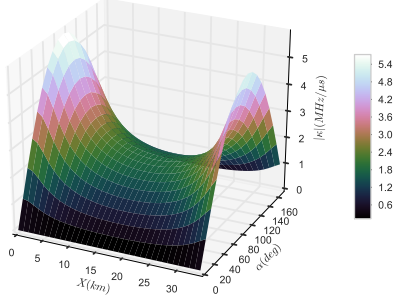


Figure 1: Dependence of chirp rate on the distance from the receiver to the shower core at shower max and also the angle between the shower direction and a line joining the receiver to shower max, from geometric considerations only.

of an EAS at radio frequencies. The radial charge density of a developing EAS varies roughly with distance; within a radial distance of roughly 1 cm of the shower axis, the charge density within that shower core is sufficiently high that a radio-reflective plasma can develop. If that plasma is sufficiently long lived, it will coherently scatter radio signals in the forward direction; such forward scattered radio signals are, in principle, detectable at distances of tens of km. Straight-forward geometric considerations lead to the expectation that, since the total pathlength from 54.1 MHz transmitter→shower core→receiver typically decreases with time for a down-moving shower, the received radar echo Doppler-redshifts by approximately 50% over a period of several microseconds, resulting in a radio-frequency “chirp” with slope of order several MHz per microsecond. The chirp rate, in terms of the distance from shower to receiver, and also the relative inclination angle of the shower is a strong function of geometry, as illustrated in Fig. 1.

The chirp can be characterized by several parameters, including the average chirp slope [MHz/s], the rate of change in the chirp slope (i.e, the time derivative of the slope [MHz/s/s]), as well as the initial, final, and maximum detectable chirp rate values. As illustrated in Figure 2, the change in the chirp slope is also tightly coupled to event geometry, as expected, so that the event geometry can, to some extent, be constrained by the observed chirp parameters.

1.1. Paper Outline

This paper is structured as follows. We first outline the general features of the expected signal character-

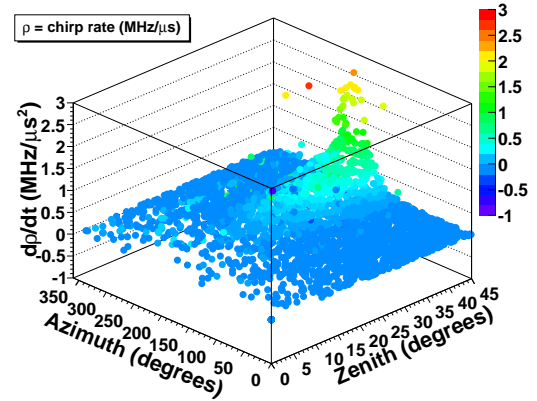


Figure 2: Dependence of time-derivative of chirp rate (shown in both color scale and vertical axis) as a function of incident cosmic ray geometry for a large number of Monte Carlo simulated radar echoes. In the Figure, the azimuthal angle $\phi=0$ is defined by the line between the transmitter and receiver; θ is the conventional shower zenith angle.

istics, which form the basis for our Monte Carlo simulations. We then review the evolution of the TARA project, with particular attention given to the remote station concept and hardware details. The performance of the current two-station configuration, including a local calibration source is then described, concluding with a prospectus for the future.

2. Chirp Simulation

To characterize the expected signals, the TARA remote station data is simulated [5, 6] by accounting for the effects of the shower properties and event geometry, atmospheric properties including local gas density, and the characteristics of the receiving antenna. Once the primary energy and the geometry are specified, the shower properties (such as shower maximum - X_{max}) are derived from the Gaiser-Hillas prescription[7]. The radio cross-section of the shower (RCS) is affected by the event geometry, and is modeled as a thin wire with a radius of order 1–2 cm. The length of the wire is governed by the plasma charge density[8]. The induced plasma charge density and lifetime, in turn, are determined by several effects, the strongest of which are collisional damping of the plasma electrons with atmospheric molecules, and attachment of the plasma electrons to oxygen molecules through two and three-body attachment mechanisms[6, 9]. Accounting for these effects at typical air shower altitudes yields plasma lifetimes of 10-100 ns.

The radiation patterns of the receiving and transmitting antenna arrays are incorporated into the simulation after careful field and anechoic chamber measurements of both the angular orientation and frequency dependence[6]. The phase and amplitude of the transmitted 54.1 MHz carrier are tracked, and updated once the observable RCS of the air shower enters the Fresnel zone of the transmitter-receiver system. The frequency evolution of the reflected signal is also directly tracked, based on the non-relativistic change in path length from transmitter to shower core to receiver.

2.1. Performance Estimate from Simulations

To derive event parameters such as zenith angle, a neural network analysis has been built around the output waveform properties. The power of the reflected signal versus time is governed by the development of the RCS and the bi-static radar equation, which is then modulated by the phase to produce the final waveform in the receiver. The simulation predicts 100-1000 cm² for the RCS, depending on parameters like the zenith

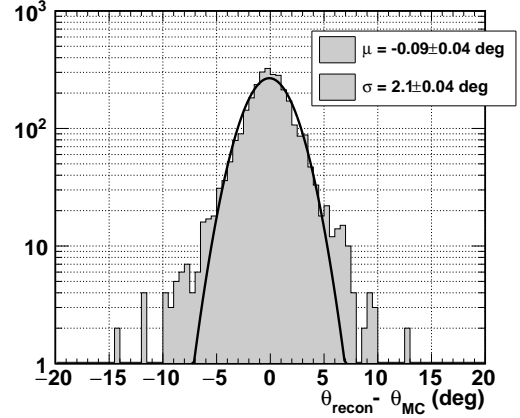


Figure 3: Difference between MC truth zenith angle, θ_{MC} , and the reconstructed zenith angle θ_{recon} , after the neural network is trained. There are 80 0.5 degree width bins in the plot.

angle, and the carrier incident angle with respect to the thin wire. To provide a realistic sampling of potentially detectable air showers, three thousand Telescope Array surface detector (SD) events were passed as inputs to the chirp simulation, which requires zenith angle, azimuthal angle, and energy.

The simulated chirp waveforms are then de-chirped as in the remote stations (delaying a copy and mixing to find low-frequency monotone, as detailed below). The chirp rate, maximum voltage, most powerful frequency, and chirp rate derivative, as measured by a single simulated station with vertical and horizontally polarized receivers, were tracked versus time for each event. Those parameters are passed finally to a 30-node by 4-layer neural network, with, e.g., in the case of Fig 3, the target parameter being the shower zenith angle. The neural network uses the Levenberg-Marquardt training technique, and attempts to minimize the mean-squared error between Monte Carlo truth and network output, using between 40-80 percent of the data to train. The final error (deviation between input and reconstructed zenith angle) histogram is shown in Fig. 3, and the width of this histogram varies from 2° – 3°, when the percentage of the data used for training is adjusted from 40-80 percent, respectively. The Gaussian fit to the results indicate little systematic bias, and that degree-level precision is available with one station, reading out both Vertical as well as Horizontal polarizations.

3. TARA Development Timeline

Initiated in 2011 with a 2 kW transmitter, TARA upgraded to a 40-kW transmitter in 2013, operating at a carrier frequency of 54.1 MHz. Within the last two years, concerted studies of background and calibration of performance have been conducted and documented[6], using the primary receiver system located at the site of the Telescope Array fluorescence detectors.

To enhance the sensitivity of TARA, at a location largely free of episodic impulsive backgrounds, we have designed and deployed two solar-powered, autonomous remote stations (RS), each operating with a power draw of approximately 15 Watts. Each remote receiver station is designed to detect chirp echoes with signal to noise ratios (SNR) as low as -10 dB.

4. Remote Station Design

The remote stations combine a custom front-end antenna with a custom data acquisition system, with separate logic for event triggering and waveform capture. Each station also includes both a power source as well as the capability to broadcast captured data back to the primary Telescope Array fluorescence detector site via a GHz communications data link.

The first element of each RS is the front-end Log Periodic Dipole Antenna (LPDA), with outputs separately for VPol and also HPol signal. Beyond this, each RS comprises five basic components: the Mixer Module to translate an input chirp signal into a triggerable monotone, the Chirp Acquisition Module (CAM) to record input chirp waveforms having sufficiently high Signal-to-Noise Ratio (SNR), a Transient Detector Apparatus (TDA, which simply registers the number of excursions over a ten-second interval above a pre-set voltage threshold) to provide simplified threshold-crossing information for the input signals, and two slow-control devices, including the IVT (Current Voltage Temperature) Board and the overall System Health Monitor (SHM) electronics. An RS block diagram is presented in Fig. 4.

Development of the RS system was completed in three stages: i) installation of RS-1 on June 28, 2014 at latitude=39.2427 N, longitude=113.0896 W, approximately 5 km from the main Telescope Array fluorescence detector site (Fig. 5), ii) installation of RS-2 on November 28, 2014 approximately 60 m displaced to the southeast of RS-1, and iii) installation of a local Chirp Calibration Unit (CCU; Fig. 6) to provide a continuous calibration source, on January 19, 2015, located

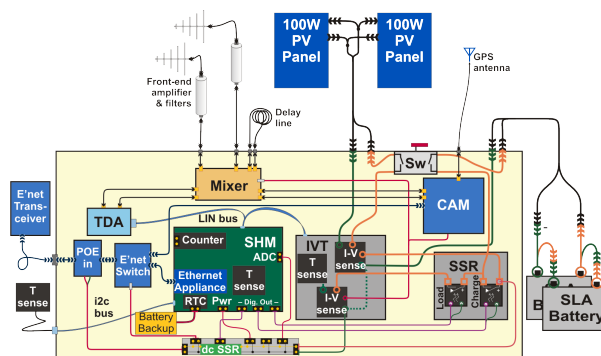


Figure 4: Block diagram showing the different components of the TARA RS detectors.

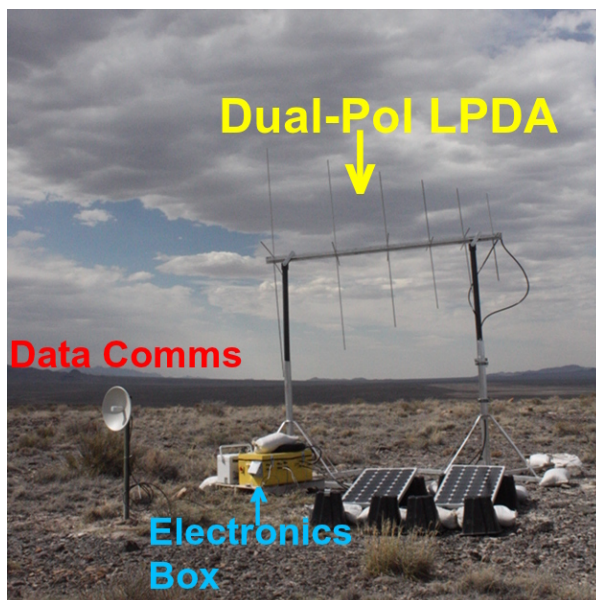


Figure 5: Remote Station-1 (RS-1), prior to displacing the electronics box from the LPDA.



Figure 7: RS-1 (right) and RS-2 (left).

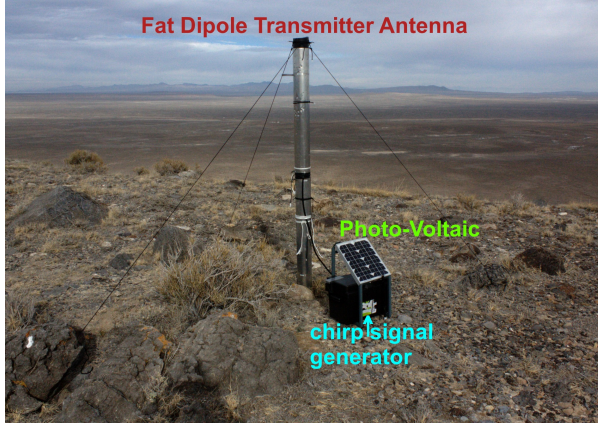


Figure 6: Chirp Calibration Unit (CCU), showing the fat dipole used as a transmitter antenna, and fixed in place with guy wires, plus the photovoltaic (PV) panel powering the chirp signal generator (in box below PV).

roughly half-way between RS-1 and RS-2. Fig. 7 shows the two remote stations in their final configuration, with RS-2 to the left; note the displacement of the antennas from the electronics boxes, to suppress locally generated noise, relative to the original configuration of RS-1. The expected azimuthal angular resolution for reconstruction of distant point sources follows from the absolute timing resolution in each of the stations, which is achieved by counting the number of clock ticks of the local 200 MHz clock in each FPGA from the local pps (pulse per second) GPS signal (with a resolution of ≈ 10 ns) to the time of the trigger latch, which is therefore discretized in 5 ns bins. The overall timing resolution is therefore of order $\sqrt{2} \times \sqrt{(10 \text{ ns})^2 + (5 \text{ ns})^2}$, or about 16 ns, corresponding to an angular resolution of order 3m/60m, or 3 degrees in azimuth. Although this is of the same order as the beam width, it is, nevertheless, suffi-

ciently small to discriminate backgrounds arising from outside the effective signal volume.

A discussion of the front-end antenna, including design, modelling and calibration has been presented elsewhere[6], therefore the remainder of this paper consists of a survey of the remaining components, in sequence, with performance benchmarks presented, where possible.

4.1. Mixer Module

Before triggering, the raw input signals must be frequency-filtered and amplified in order to suppress known backgrounds (e.g., the known FM band) and also to ensure that the signal strength is comfortably within the dynamic range of the signal digitizer. The Mixer Module therefore includes splitters (ZMSC-4-1-BR, Mini-Circuits), filter (SLP-1.9+, Mini-Circuits), amplifier (ZFL-500LN+B, Mini-Circuits) and bias tees (ZFBT-4RG-FT, Mini-Circuits) as shown in Fig. 8.

The mixer module also includes a Mini-Circuits ZX05-1L-S+ mixer, which is crucial to the identification of putative UHECR-induced radar echoes. As detailed elsewhere[6], the EAS-reflected chirp signal can be characterized by a duration T_c seconds, a time-varying Amplitude $A(t)$ having with start phase ϕ_0 , start frequency f_0 , stop frequency f_1 and chirp rate κ Hz/s. Both up and down chirps are treated the same in the detector and have equal triggering efficiency. An example of a signal of interest is shown in Fig. 9. Assuming that it is centered around time $t=0$, such a chirp signal has the form, in terms of the parameters above,

$$s(t) = A(t)\sin(\phi_0 + 2\pi f_0 t + \pi \kappa t^2) \quad (1)$$

4.1.1. De-chirping

We have employed an analog detection scheme (“de-chirping”) designed to detect the presence of the signal

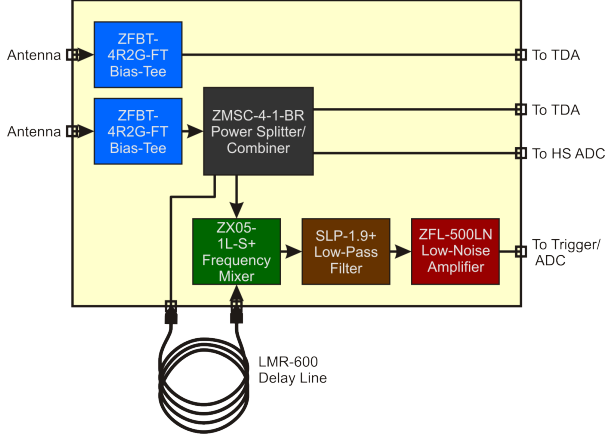


Figure 8: Block diagram showing the different components of the mixer module.

$s(t)$ without prior knowledge of the chirp rate κ . In the first step, the signal is down-converted to a monotone. To achieve this, the signal is mixed with a delayed copy of itself, i.e $s(t) \otimes s(t - \tau)$, with $\tau \sim 100$ ns, as depicted in the radar block diagram in Fig. 10.

For an incident chirp signal, the non-linear components in the mixer result in a product term that yields a monotone at a beat frequency

$$f = \kappa\tau, \quad (2)$$

where τ is the delay time. This delay is created with a short length (~ 30 m, selected as a length which results in destructive interference between the direct and time-delayed 54.1 MHz large-amplitude carrier signals, which would otherwise obscure the chirp) LMR-600 cable, which produces negligible losses. This is illustrated in Fig. 11, in which a -10 MHz/ μ s chirp is down-converted to a 1 MHz monotone. The 1 MHz monotone can then be detected using a simple threshold-crossing criterion, in which case a trigger is generated and waveform-capture initiated.

4.2. Triggering Scheme

The expected value of chirp slopes from EAS echoes are typically between -10 to -1 MHz/ μ s. Consequently, and based on the previous discussion, a 100 ns time delay between the initial input signal and the delayed copy results in a down-converted signal with frequency between ~ 100 kHz and 1 MHz. To trigger on such signals, it is advantageous to split the mixed signal into multiple copies, each of which is then passed through a distinct band-pass filter and a subsequent envelope detector. Different frequency bands are then compared by

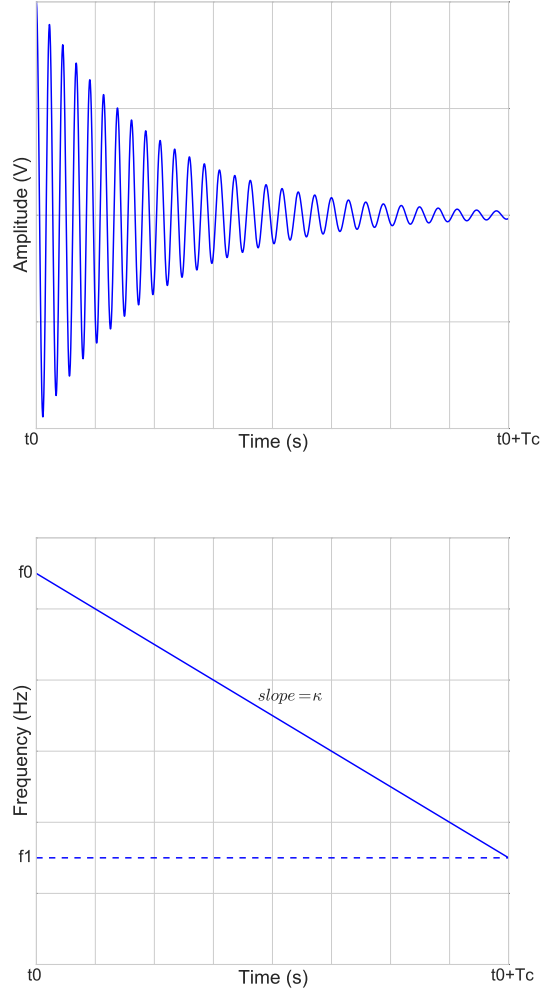


Figure 9: A linear down-chirp with changing amplitude in the time domain (top) and frequency-time domain (bottom).

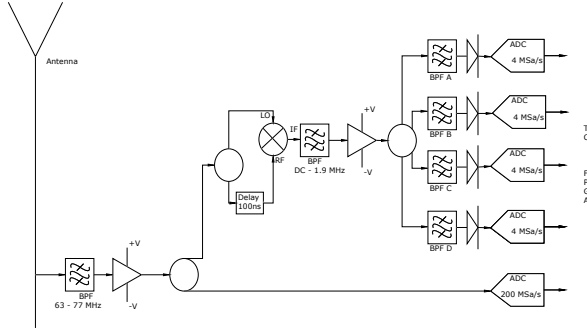


Figure 10: Radar block diagram illustrating the down-conversion process along with filtering and enveloping.

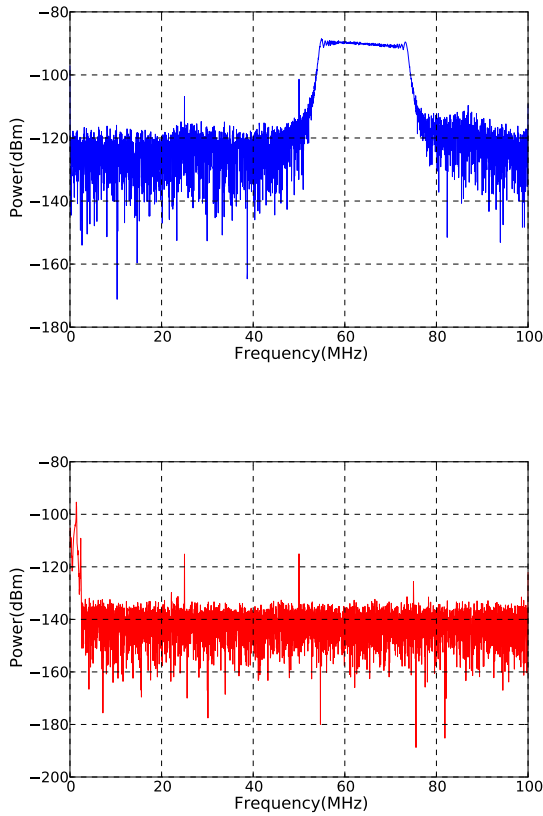


Figure 11: Top: power spectrum of $-10 \text{ MHz}/\mu\text{s}$ chirp created by a laboratory signal generator, prior to mixing. Bottom: power spectrum of monotone signal after signal mixing and low-pass filtering. The chirp is evident as the left-most peak in this distribution at $\sim 2 \text{ MHz}$. Higher-frequency overtones are suppressed in the triggering logic by bandpass filtering.

majority logic in an FPGA, requiring a trigger criterion of no more than two adjacent frequency bands above threshold. This trigger criterion is designed to suppress broadband impulsive noise, which will typically fire all four bands.

Fig. 12 (captured on an oscilloscope) illustrates the triggering scheme using a signal generated in the lab. After mixing and filtering, the signal is then passed through an envelope detector (8471D; Agilent, Inc.). Here, a chirp with 0 dB SNR with slope $-1 \text{ MHz}/\mu\text{s}$ is first band-pass filtered (41–100 MHz) and then amplified by 20 dB. The signal is then mixed and low-pass filtered (DC–1.9 MHz) and passed through the Agilent power detector.

4.3. Chirp Acquisition Module (CAM)

The CAM is an embedded system with a modular design that provides hardware and software integration for chirp detection and waveform capture. It is composed of five basic parts: a Trigger Board, High Speed Board, an FPGA, a GPS unit and a Single Board Computer (SBC), as shown in Fig. 13. A description of each of these sub-systems follows.

4.3.1. Trigger Board

As the frequency of the de-chirped monotone is directly related to the signal chirp rate, that monotone is band-passed into four distinct frequency bands prior to discrimination. This is done to both ensure that the chirp rate is within a range commensurate with that expected for a cosmic ray, as well as to obtain a first estimate of the chirp rate itself.

A trigger signal is asserted only if the monotone power, as measured by the envelope detector, exceeds some adjustable, pre-set threshold T_0 . The envelope detector includes a rectifying diode, followed by an RC combination that allows the output waveform to follow the envelope of the signal. The output of the four band-pass filters are then passed into the ADC (ADC 80066, Analog Devices)[10]. The ADC is powered from a 5 V power supply, typically consuming 490 mW of power, and is packaged in a 28-lead Small-Shrink-Outline-Package (SSOP). The ADC is operated in the Sample and Hold Amplifier (SHA) mode with the 16-bit output multiplexed into 8-bit words and accessed in two read cycles clocking at 4 MHz per channel. The ADC register is programmed via the Serial Peripheral Interface (SPI) at 24 MHz. Finally, the data are transferred via the FPGA pmod inputs for triggering (see Sec. 4.3.3). Along the signal path, differential signaling is used to provide superior common-mode noise rejection.

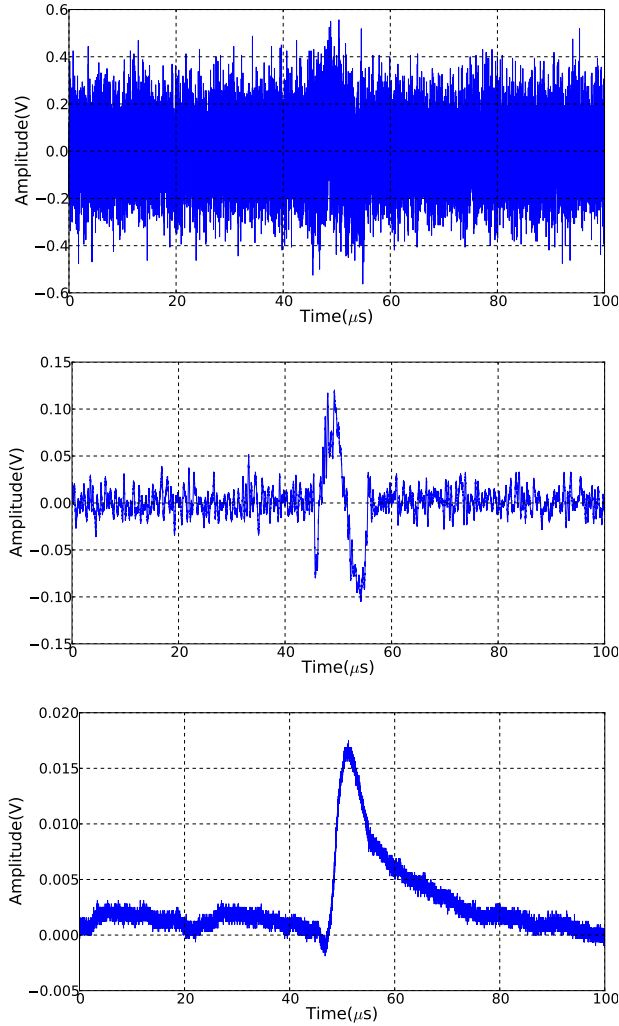


Figure 12: Top: A 0 dB SNR and 1 MHz/ μ s chirp embedded in noise prior to de-chirping. Middle: The monotone signal after input chirp is mixed with the delayed copy of itself and passed through a low-pass filter. Bottom: Resulting monotone passed through the Agilent 8471D power detector.

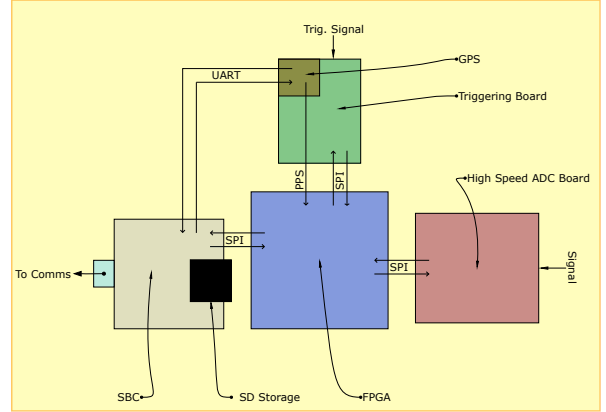


Figure 13: Elements of the CAM unit illustrating the communications protocols.

4.3.2. High Speed Board

The TARA High Speed Board is a commercially available Analog Devices AD9634 Evaluation Board[11]. The board, capable of sampling up to 250 MHz ADC with a total power consumption of 360 mW, affords 12-bit resolution. The ADC is clocked at 200 MHz and uses an 1.8V SPI port at 24 MHz for register programming and read back.

The 12 bit words are transferred using a custom adapter between the Evaluation Board's LVDS (Low Voltage Differential Signaling) parallel output port and the VHDC (Very High Density Cable) connector on the FPGA.

4.3.3. FPGA

We now provide details on the FPGA (Nexsys 3 digital system development board using the Xilinx Spartan 6 FPGA) timing, generated with an FPGA board (Nexsys 3 using a Xilinx Spartan 6 FPGA, Digilent). To configure the FPGA, the configuration file is first stored in a non-volatile parallel PCM (Phase Change Memory) device and then transferred to the FPGA on power-up using the BPI-UP port. This is one of four possible configuration modes on the development board, and is achieved by removing all connections on the J8 jumper[12].

The Nexys3 board includes a single 100 MHz CMOS oscillator connected to pin V10 (the GCLK0 input in bank 2). PLL (Phase Locked Loop) and DCM (Digital Clock Manager) features on the board can be used to synthesize other frequencies. A Xilinx Clock Gen wizard is correspondingly used to synthesize a 48 MHz clock. These are then further sub-divided to synthesize clocks for transfer and synchronization between periph-

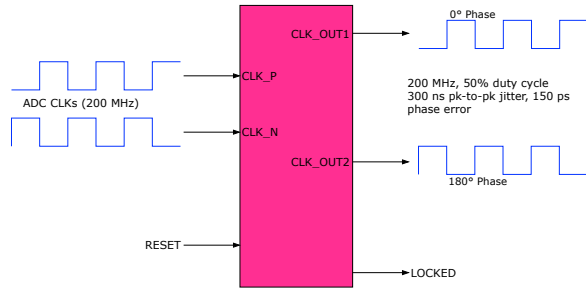


Figure 14: High Speed Board's 200 MHz differential clocks and Xilinx ClockGen wizard used in synthesizing out-of-phase 200 MHz frequencies.

eral boards, as well as other requisite functions.

The triggering board is connected to the FPGA development board via the pmod connector. These pmod connectors are 2x6 right-angle, 100-mil female connectors that mate with standard 2x6 pin headers, with each set of 12 pin pmod connectors comprising two 3.3V VCC signals, plus two ground signals and eight logic signals.

Words from the triggering board are de-serialized from the parallel input ports in the FPGA via the implementation of a Finite State Machine (FSM). Once shifted in, a comparator is invoked and the trigger logic queried.

In order to regularly monitor the environment, a “forced”, or snapshot trigger is also implemented on 0xFF clock cycles of the GPS pps (pulse per second) clock. This corresponds to a typical time interval of 4.25 minutes between forced triggers.

All I/Os to the VHDC connector are routed as matched pairs to support LVDS signaling, powered at 2.5V; all FPGA pins routed to the connector are located in FPGA I/O bank0. There are 20 matched pairs of data signals, 20 ground signals and 8 power signals on the VHDC connector [12].

The 200 MHz differential clock outputs from the High Speed Board are brought into the FPGA and used in frequency synthesis, via the Xilinx ClockGen Wizard, using two clocks at 200 MHz, aligned such that one is 180 degrees out of phase with the other (see Fig. 14).

The AD9634 ADC sends even/odd bits on the rising/falling edge of the sampling clock. A DDR (Double Data Rate) interface [13] is used between the FPGA and the ADC. The bits are aligned per the C0 non-inverted clock, synthesized by use of an extra flip-flop.

IBUFDS (Input BUFfer Differential Signaling) is a differential I/O primitive [13] that is instantiated for the signals from the ADC and have two pins, corresponding

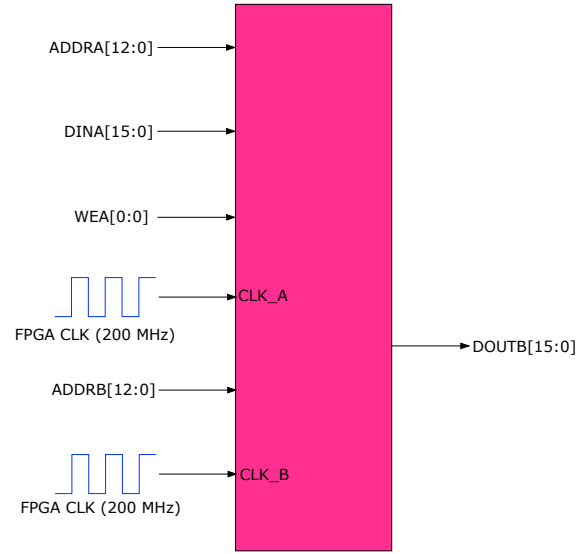


Figure 15: Xilinx Block Memory Generator Signals.

to the P and N channels of the differential signal.

Bits are then serialized via an FSM and stored in a circular buffer with a RAM depth of 2^{13} (8192) words and width of 16 bits (the actual width is 12 bits but the buffer is padded with four bits; bits 0,7,8,15 are redundant) that are continuously written and read at 200 MSa/s. The Xilinx Block Memory Generator Wizard handles the writing, reading and memory management, employing one 9K BRAM and seven 18K BRAMs (see Fig. 15).

For each trigger, the 16 bit words (2^{13} [8192] bit depth) are written into a FIFO at 200 MSa/s and then read out at 8 MSa/s (SBC's SPI clock).

In addition to the signal captured by the FPGA from the High Speed Board, the triggering information is also saved. This information forms the header of the data to be transferred.

The threshold level for triggering is set via a Raspberry Pi[14] SBC (described below) using a chip select line; the aforementioned data to the SBC are transferred using the same data line, but a different chip select is activated once an interrupt is initiated on the FPGA side. This interrupt is ideally initiated when the FIFO buffer is full; however, due to latencies arising due to the crossing of clock domains in the FIFO, three D synchronous flip-flops, as shown in Fig. 16, are instantiated after the assertion of “full” on the FIFO, and therefore before the interrupt is asserted. An FSM controls the transfer logic between the FPGA and SBC.

In all transfers to/from the SBC(Master) and

FPGA(Slave), serial peripheral interfaces are used and clocked at 8 MHz (see Fig. 17).

4.3.4. GPS

The GPS unit (i-Lotus M12M)[16] for event time-stamping is mounted on the Triggering Board for stability and convenient powering. The UART communications protocol is used to transfer data from/to the SBC. The GPS PPS (Pulse Per Second) is used as a counter to obtain forced triggers as described earlier in Sec. 4.3.3. The functional Block diagram of the GPS to SBC and FPGA connections are shown in Fig. 18. Timing information is periodically queried from the GPS unit and used to update the time base on the SBC.

4.3.5. Single Board Computer (SBC)

The Single Board Computer used in the CAM is the commercially available Raspberry Pi Model B Rev. 2 (Rpi - B rev 2.). The RPi uses the Broadcom BCM2835 SoC (System on Chip) that includes the ARM1176JZF-S 700 MHz processor, VideoCore IV GPU, 512 MB RAM and access to other I/O peripherals, as well as a separate three port USB Hub.

The RPi has a 26 (2×13) pin 2.54 mm expansion header with 8 GPIO (General Purpose Input/Output) pins and dedicated peripherals such as SPI, and UART, along with 3.3V, 5V and GND supply lines. The board includes a 32 GB SD card to which data are stored and also where a minimal Raspbian Wheezy (118 MB image) is compiled with hard float support (3.6.11+ hardfp kernel). WiringPi[15] written in C for the BCM2835 provides access to the GPIO and the Adafruit Prototyping Pi Plate provides convenient pin access to connect with the FPGA and GPS unit (see Fig. 19).

4.4. System Monitoring and Powering

In addition to the CAM, the Chirp Detection Station includes several components to power the station and monitor environmental variables. These components are the Transient Detector Apparatus (TDA) Board, the

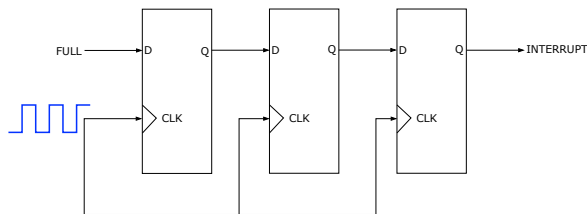


Figure 16: Implementation of D Flip Flop to assert an Interrupt signal.

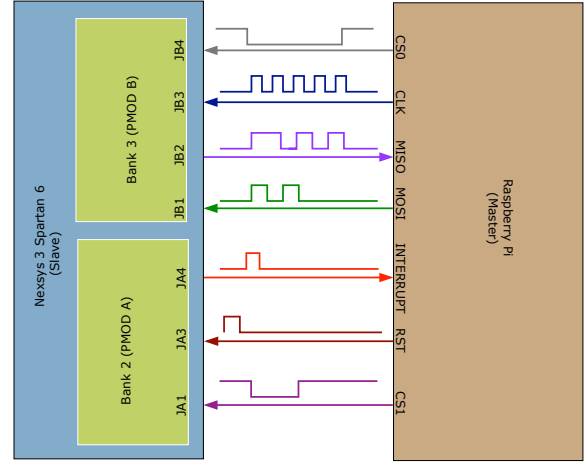


Figure 17: The FPGA-SBC Interface.

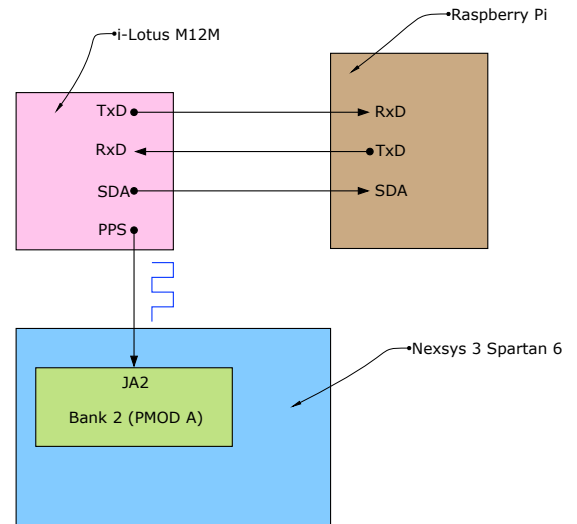


Figure 18: GPS to FPGA and SBC Interface.

current voltage and temperature (IVT) board and the system health monitor (SHM). A prototype station comprising just these components had been deployed in the Summer of 2013 to acquire environmental and powering information. In the revised stations, deployed in 2014, modifications were made and the system was updated to operate in conjunction with the chirp acquisition module.

4.4.1. TDA (Transient Detector Apparatus) Board

The TDA continuously monitors ambient noise at the site by counting threshold crossings. The thresholds are set with Digital-to-Analog Converters that are remotely

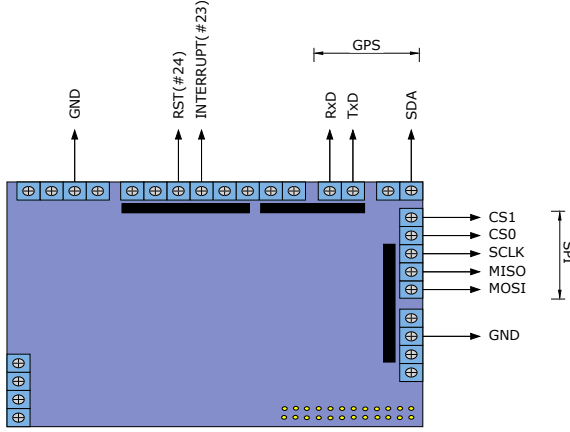


Figure 19: Ardafruit Prototyping Pi Plate showing the corresponding GPIO pins to the FPGA and GPS units.

controlled through the System Health Monitor (SHM). The measurement period, usually 10 seconds, is also controlled from the SHM. Prior versions, including that deployed in the prototype station, had a front-end amplifier in addition to a log amplifier, however both have been removed in subsequent iterations, and amplification now resides in the Antenna front-end. A functional block diagram of the TDA is shown in Fig. 20. A serial network protocol (LIN ["Local Interconnect Network"] - bus) connects the TDA to the SHM.

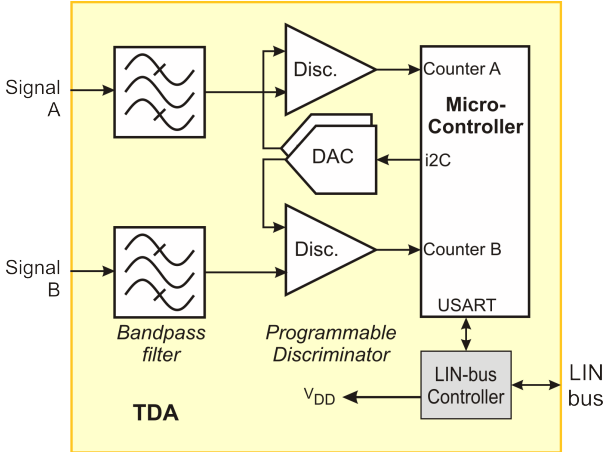


Figure 20: Transient Detector Apparatus (TDA).

4.4.2. IVT (Current, Voltage and Temperature) Measurement Board

The IVT board consists primarily of current sensors, allowing voltage measurement and monitoring of the

PV (Photo Voltaic) panels. It has the capability of measuring current and voltage for a wind turbine, however this has not been installed at present. In addition, the board includes temperature sensors along with the current and voltage sensors, all of which feed into a microcontroller. A functional block diagram of the IVT board is shown in Fig. 21. As in the TDA, a LIN-bus connects the IVT board to the SHM.

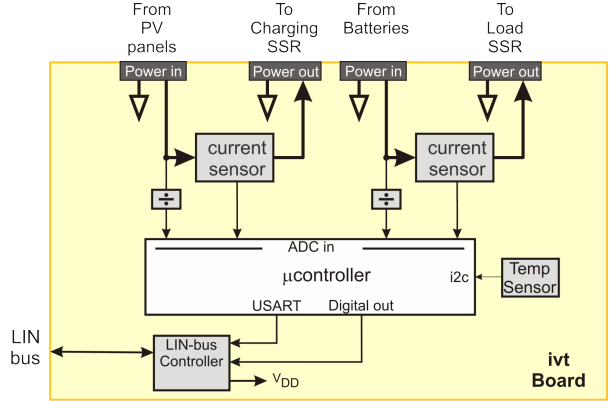


Figure 21: Current Voltage Temperature (IVT) Board.

4.4.3. SHM

The System Health Monitor reports on the environmental and operational status of the Chirp Detector. This consists of a LIN bus connection to the TDA and IVT board, where ambient noise, PV current and voltage are measured. Additional temperature sensors measure the temperature both inside and outside the detector. The SSR's (Solid State Relays) are controlled via the SHM; using an Ethernet appliance, the status of the detector is reported on a web page. Operational characteristics of the detector are controlled via a CPLD (Complex Programmable Logic Device) with the environmental data stored onto an SD card. A functional block diagram of the SHM is shown in Fig. 22.

The SHM has five adjustable threshold levels that dictate when communications, loads and charging are turned on/off (Fig. 23). To avoid over-charging, e.g., there is a failsafe such that a low-resistance, and therefore high-dissipation load is swapped into the system in the unlikely event that the system power demand is unable to draw normal charge from the batteries.

4.5. Chirp Calibration Unit (CCU)

In order to calibrate the remote stations independently, a Chirp Calibration Unit, with signal characteristics similar to those of an expected cosmic-ray induced

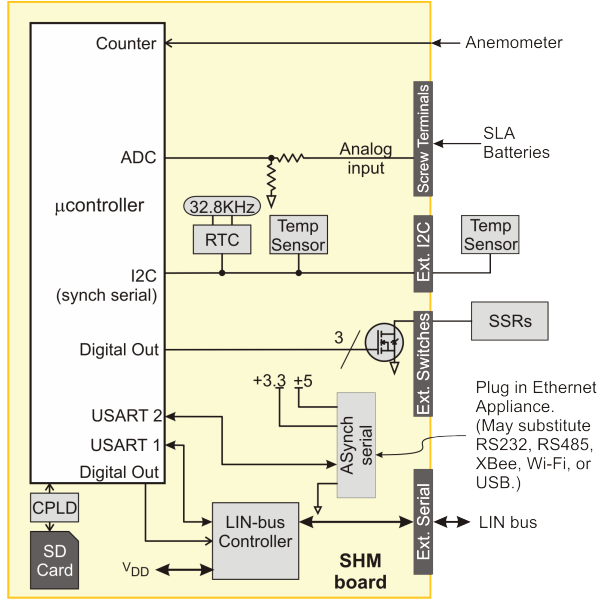


Figure 22: System Health Monitor (SHM).

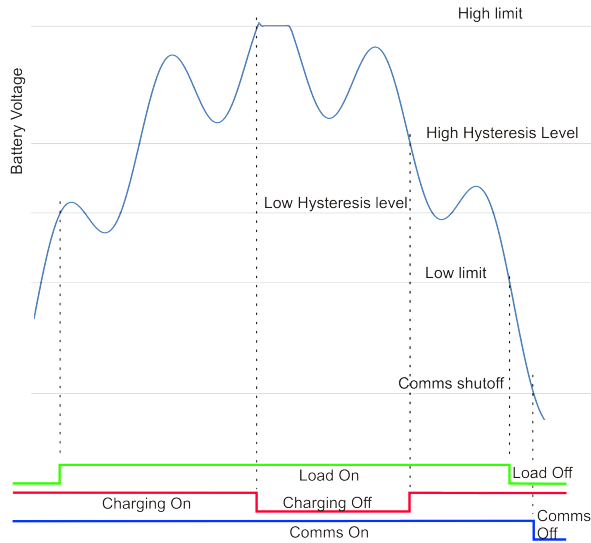


Figure 23: Threshold Settings on the System Health Monitor (SHM).

chirp, has been deployed in the field. This unit is depicted in Fig. 24, and comprises a 'fat - dipole' transmitter antenna plus an Arduino controlling an SSR for the Signal Forge sf1020 signal generator.

The dipole was initially tuned to a frequency of 70 MHz, however, in order to transmit a broadband chirp-like signal, the radius of the dipole was re-optimized to efficiently transmit at 55 MHz. Stable 1 pps chirps spanning 80 MHz→50 MHz and 20μs duration over a

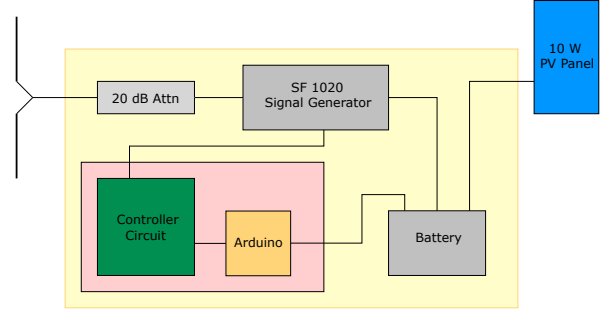


Figure 24: Schematic of the Chirp Calibration Unit (CCU).

period of 10 seconds are generated every 2 hours. The calibration unit was placed ~45 m from the two remote stations to give high SNR chirp signals (20 dB SNR). A spectrogram of a calibration chirp is shown in Fig. 25

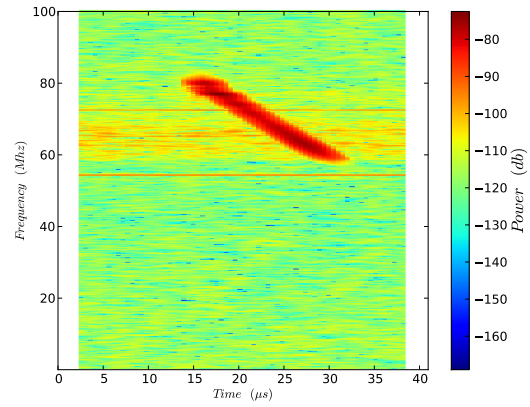


Figure 25: CCU-triggered chirp as detected by RS-2.

5. Deployment and Initial Performance

The initial deployment of RS-1 in June, 2014 was followed by an upgrade of RS-1 and also field deployment of RS-2 in November, 2014, followed by field installation of the CCU in January, 2015. The spectrogram for the first data taken by RS-1 is shown in Figure 26. The two strongest and most persistent lines in the plot are those at 54.1 MHz (due to the carrier signal from the TARA transmitter) and one at 72 MHz which was later traced to a source in the RS-1 electronics and easily mitigated by physically moving the antenna away from the RS-1 electronics power box. The former was additionally suppressed by installation of tuned, in-line analog RLC filters in August, 2014. Absent any filtering, the 54.1 MHz carrier can saturate our amplifiers, resulting

in an overall increase of the observed noise floor over tens of MHz.

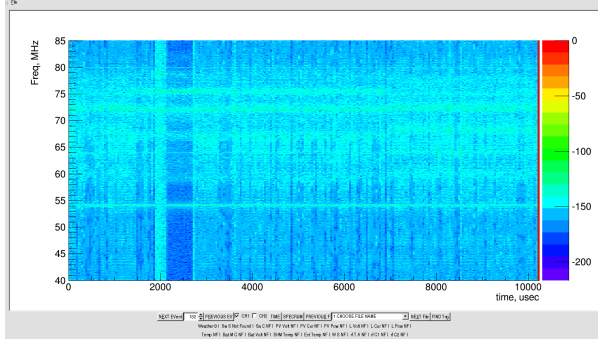


Figure 26: Spectrogram of initial RS-1 data; data taken one day after initial installation (June, 2014).

Currently, trigger rates for both stations are well below 1 Hz, and therefore allow operation at nearly 100% livetimes. Since upgrading RS-1 and installation of RS-2, our analysis has thus far focused on a verification that the ambient noise floor is approximately commensurate with expectations from a combination of thermal plus galactic noise. Figures 27 and 28 show the averaged corrected VPol power for each of the two remote

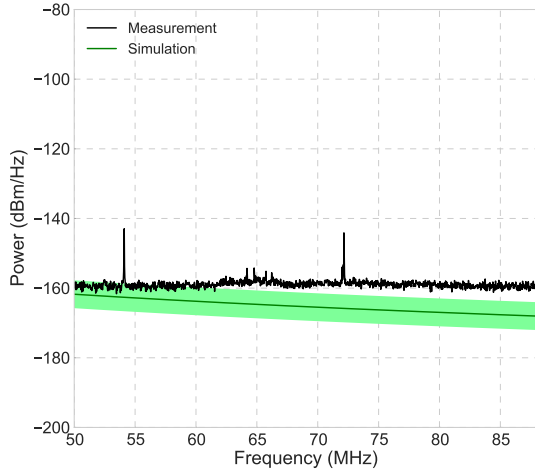


Figure 27: Measured RS1 noise floor, with estimated galactic noise overlaid in green. Data taken January, 2015.

stations based exclusively on forced triggers, respectively. Despite considerable filtering, including the custom RLC filter that provides a 24 dB deep notch over a 1 MHz bandwidth, the carrier at 54.1 MHz is still observable above the ambient background. We also observe a local 72.2 MHz source of unknown origin. Aside from

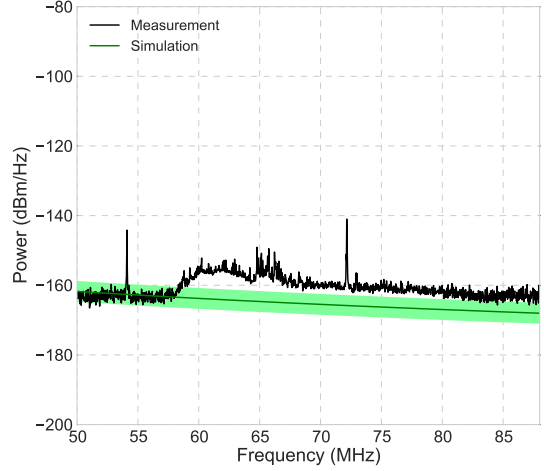


Figure 28: Measured RS2 noise floor, with estimated galactic noise overlaid in green. Data taken January, 2015.

those continuous wave (CW) lines, the ambient background is within the few dB absolute systematic error (for each station independently) of our expectation for the irreducible background in this frequency band.

The RS environment should be sufficiently radio-quiet that the sidereal variation in the environmental power, due to the motion of the galactic center across the sky, should be observable. Figure 29 shows the measured environmental power, for a 5 MHz band centered at 70 MHz, as a function of time for the first 12 days of RS-2 operation. Overlaid is a fit to that variation, as well as the known azimuthal position in the sky of the galactic center relative to boresight of the front-end log-periodic dipole antennas. As expected, the two curves are very close to each other in absolute phase.

6. Summary and Outlook

As of mid-November, 2014, the TARA transmitter has been rotated from its initial HPol configuration into a VPol configuration, designed to better match the preferential polarization from directly vertically descending showers. Data will be accumulated for approximately one year with the current TARA configuration, consisting of a National Instruments Flex-RIO-based DAQ located at the main TARA data-taking building in LongRidge, UT, plus the two remote stations described herein. As mentioned herein, the radar cross-section is directly related to the size of the reflective plasma along the shower axis (“shower core”); that plasma density is predicted by sophisticated air shower simulation

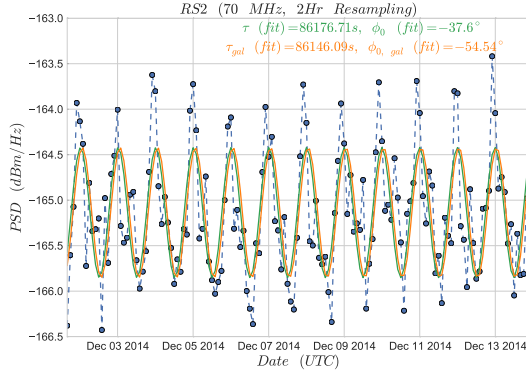


Figure 29: Variation in measured ambient environmental power (taken in a 5 MHz band centered on 70 MHz, superimposed with the movement of the galactic center in the sky. The former has been fit to a sine wave, giving agreement with the expected phase of the galactic center to within 5%.

packages such as CORSIKA. If the radar cross-section is equivalent to that predicted by CORSIKA simulations for a typical 10 EeV UHECR-induced extensive air shower, these stations should observe tens of events per month at the -10 dB trigger threshold achieved in the lab. Conversely, the lack of definitive UHECR observations via radar reflections will result in constraints on the effective air shower radar cross-section, or, alternately, the lifetime of the putative shower core reflective ionization plasma. In such a case, mechanisms such as collisional damping of the coherent plasma response due to interactions with local gas molecules, or even loss of charge in the core plasma due to recombination of plasma charge with gas molecules (likely oxygen, which has a higher electron affinity than nitrogen) may render an unfavorable outlook for the continued development of this approach in-air. Nevertheless, the technique may still offer promise for application to showers developing in solid media such as ice, as has been suggested elsewhere[17].

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